VLSI Project: Elevator Control System

Part 3

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Specs

Area: 4.055um x 1.3um = 5.252um

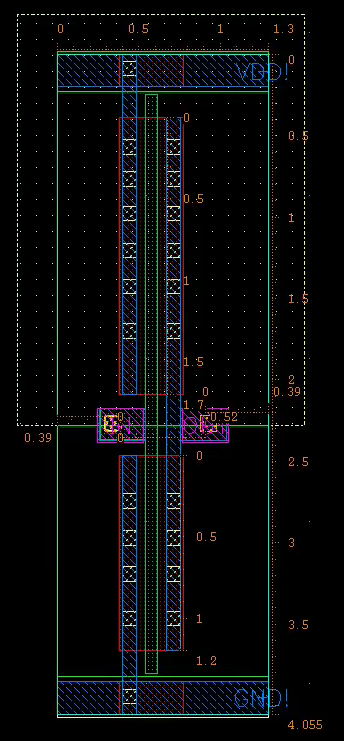
Rise Delay: 61.6ps

Fall Delay: 42.6ps

Output Rise Edge Rate: 71.4ps

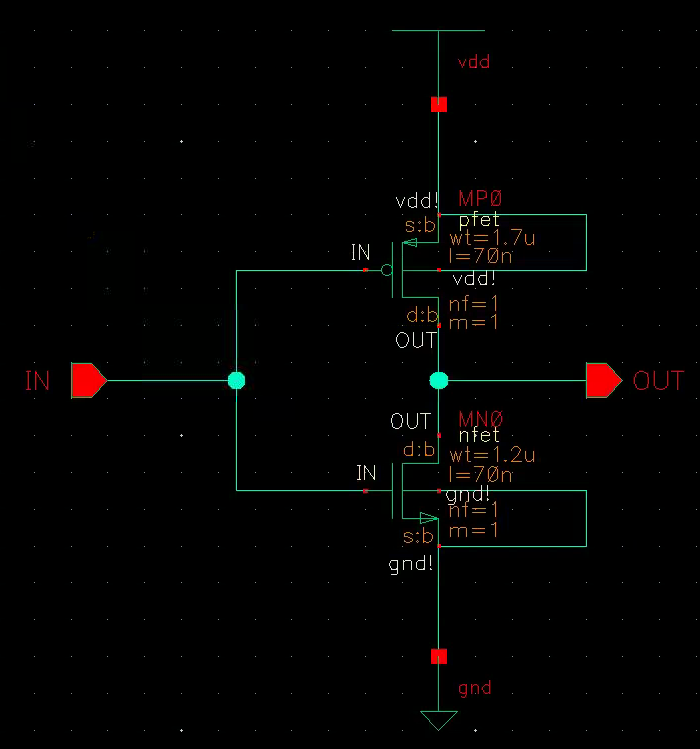
Output Fall Edge Rate: 42.4ps

**Inverter Layout Screenshot**



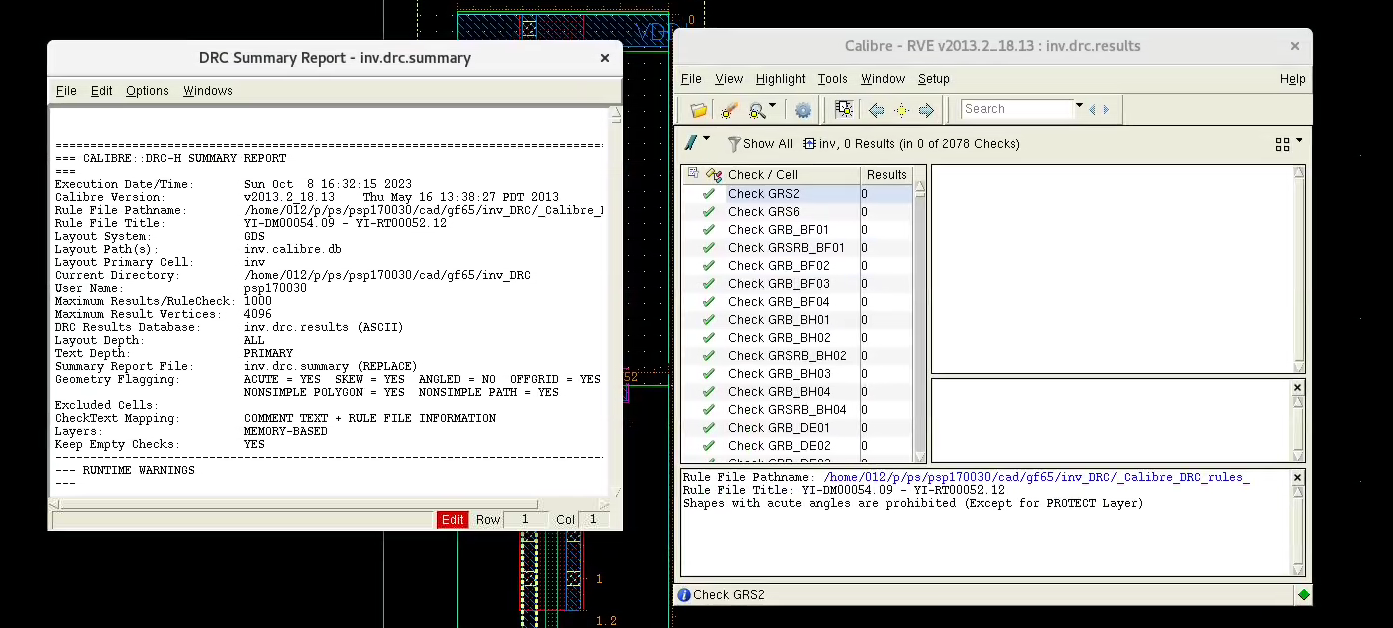
The PRBoundary is shown to be 4.055um by 1.3um. Shown by the screenshot below. The Pin Pitch is shown to be 0.52um and the Offset is shown to be 0.39um. 

**Inverter Schematic Screenshot**



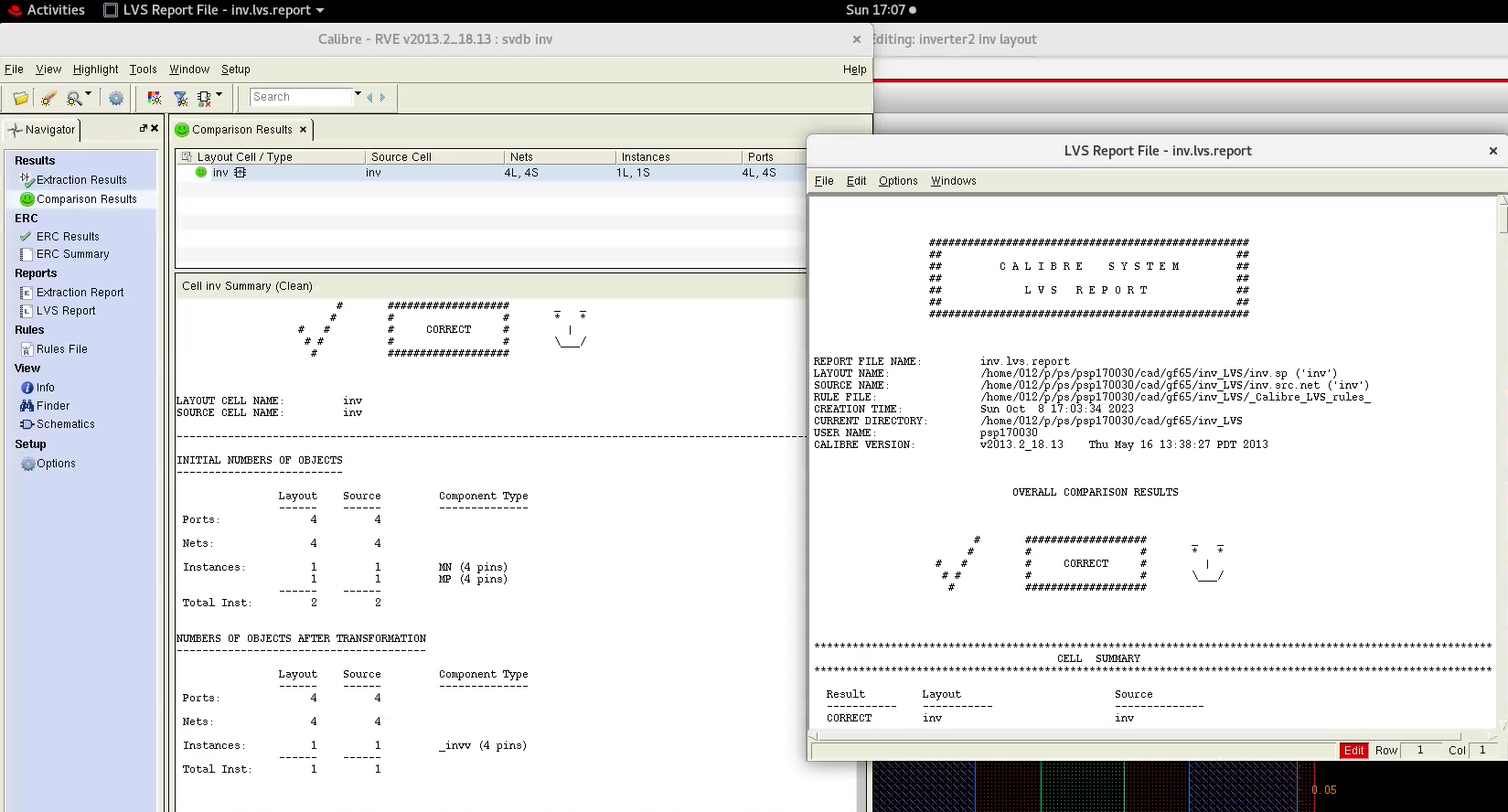
The width of the pmos and nmos FETs were set to 1.7um and 1.2um as specified for our group. The length of both FETs were set to 70nm. This was due to the error that we were seeing during the LVS check, that the lengths had to be equal at 70nm.

**Inverter DRC Check Screenshot**



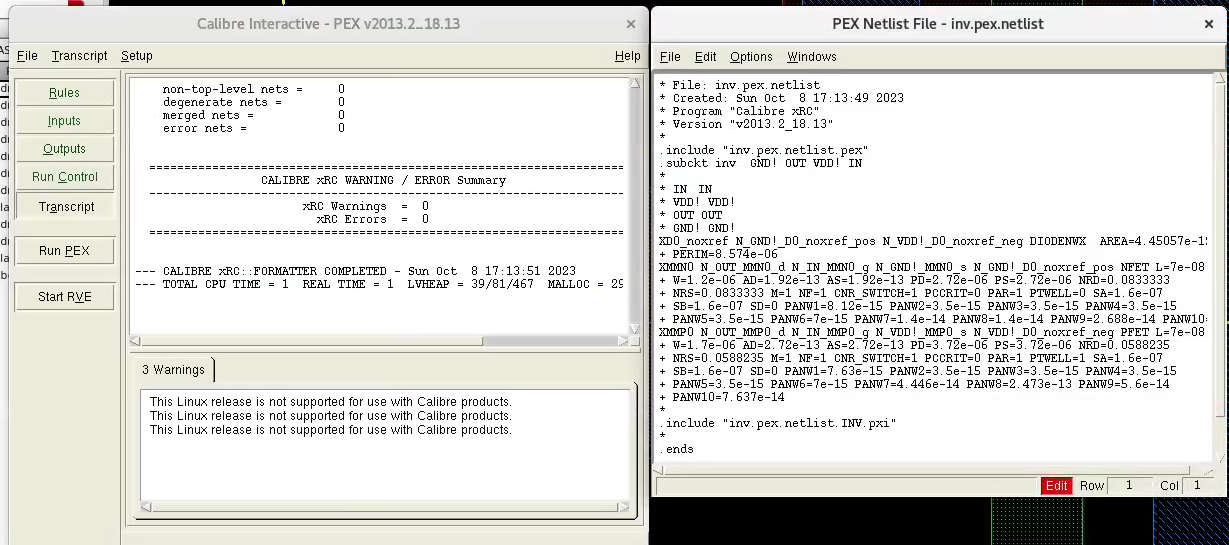
Based on the above screenshot, during the DRC, there were no results or errors found.

**Inverter LVS Check Screenshot**

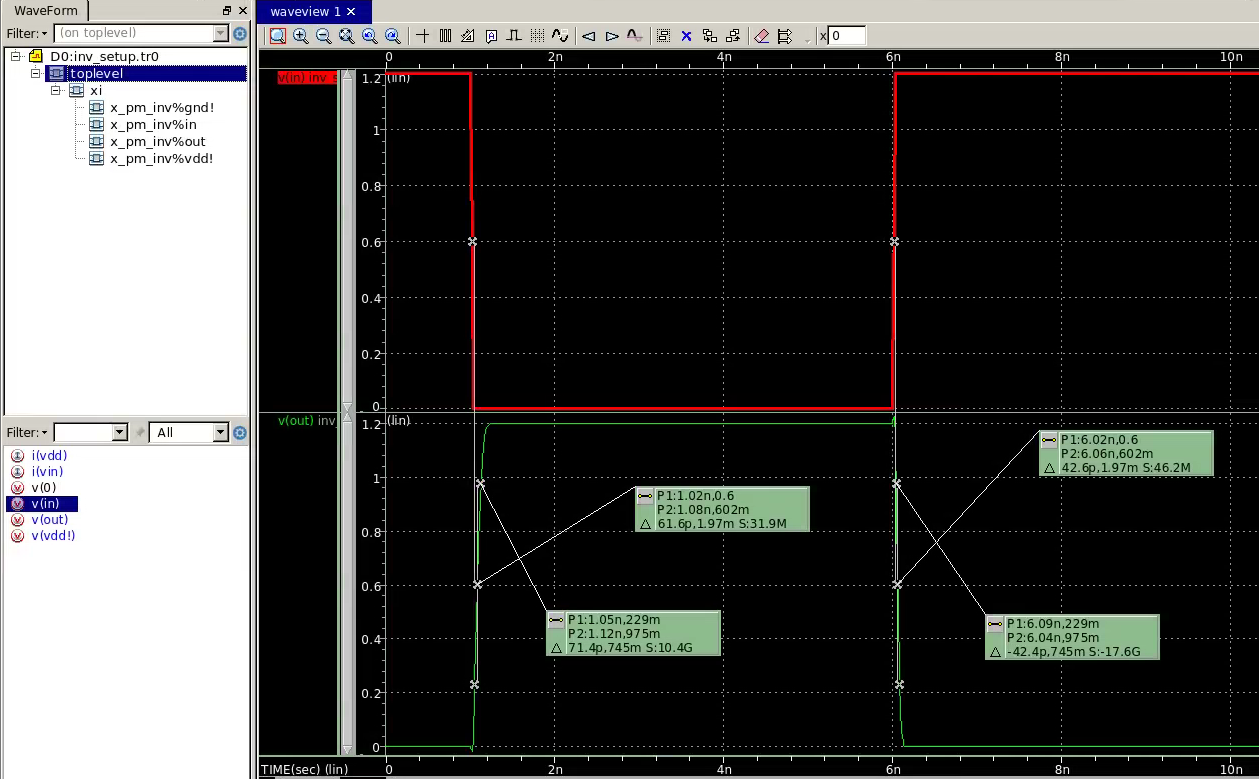


Based on the above screen, during the LVS, there were no errors found and the smiley face was displayed. One note is that we had to change the length of the FETs in the schematic to 70nm to correct an error we were seeing at this stage.

**Inverter PEX Check/Generation Screenshot**



**Waveforms**



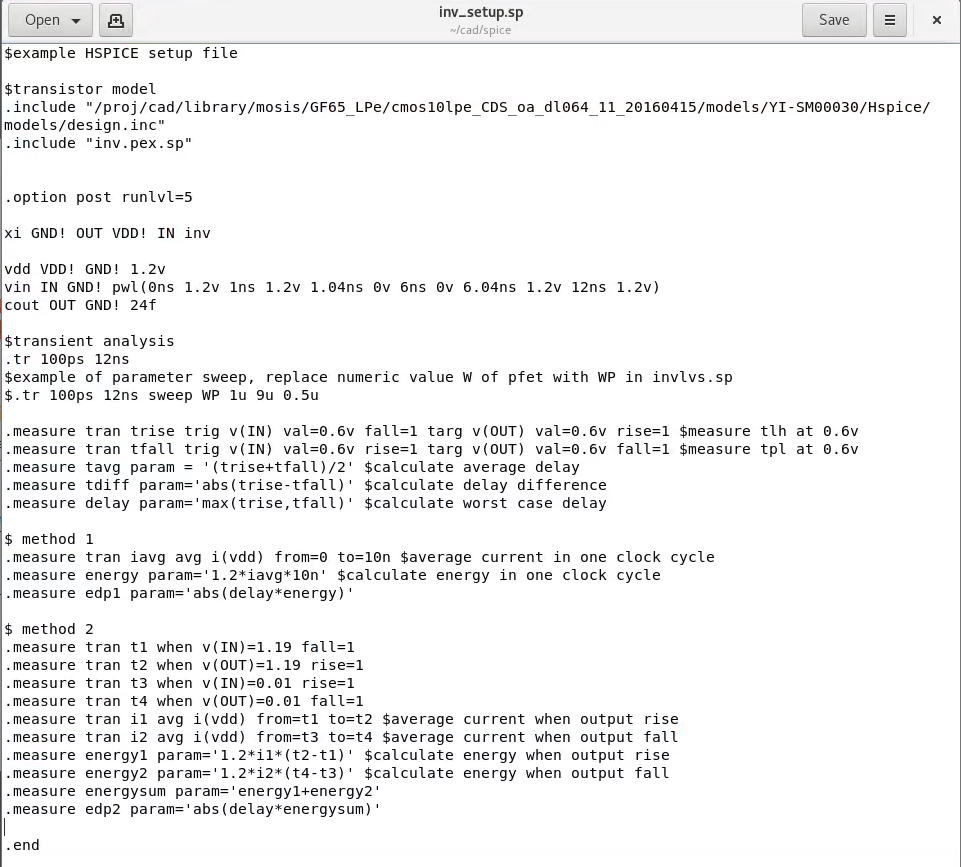
Rise delay: 

Fall delay: 

Output rise edge delay: 

Output fall edge delay: 

**Spice Test Setup Screenshot**



Above is the test setup file, with change of the slew rate to 40 ps and 24 fF for C load.

**Spice Test Setup Code**

$example HSPICE setup file

$transistor model

.include "/proj/cad/library/mosis/GF65\_LPe/cmos10lpe\_CDS\_oa\_dl064\_11\_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "inv.pex.sp"

.option post runlvl=5

xi GND! OUT VDD! IN inv

vdd VDD! GND! 1.2v

vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.04ns 0v 6ns 0v 6.04ns 1.2v 12ns 1.2v)

cout OUT GND! 24f

$transient analysis

.tr 100ps 12ns

$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp

$.tr 100ps 12ns sweep WP 1u 9u 0.5u

.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure tlh at 0.6v

.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure tpl at 0.6v

.measure tavg param = '(trise+tfall)/2' $calculate average delay

.measure tdiff param='abs(trise-tfall)' $calculate delay difference

.measure delay param='max(trise,tfall)' $calculate worst case delay

$ method 1

.measure tran iavg avg i(vdd) from=0 to=10n $average current in one clock cycle

.measure energy param='1.2\*iavg\*10n' $calculate energy in one clock cycle

.measure edp1 param='abs(delay\*energy)'

$ method 2

.measure tran t1 when v(IN)=1.19 fall=1

.measure tran t2 when v(OUT)=1.19 rise=1

.measure tran t3 when v(IN)=0.01 rise=1

.measure tran t4 when v(OUT)=0.01 fall=1

.measure tran i1 avg i(vdd) from=t1 to=t2 $average current when output rise

.measure tran i2 avg i(vdd) from=t3 to=t4 $average current when output fall

.measure energy1 param='1.2\*i1\*(t2-t1)' $calculate energy when output rise

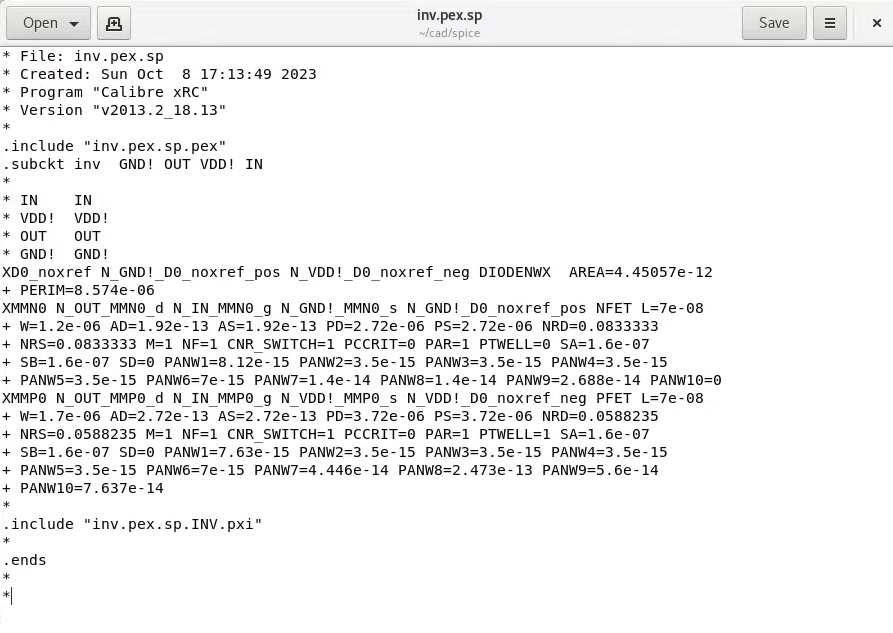
.measure energy2 param='1.2\*i2\*(t4-t3)' $calculate energy when output fall

.measure energysum param='energy1+energy2'

.measure edp2 param='abs(delay\*energysum)'

.end

**Extracted Spice Netlist Screenshot**



**Extracted Spice Netlist Code**

\* File: inv.pex.sp

\* Created: Sun Oct 8 17:13:49 2023

\* Program "Calibre xRC"

\* Version "v2013.2\_18.13"

\*

.include "inv.pex.sp.pex"

.subckt inv GND! OUT VDD! IN

\*

\* IN IN

\* VDD! VDD!

\* OUT OUT

\* GND! GND!

XD0\_noxref N\_GND!\_D0\_noxref\_pos N\_VDD!\_D0\_noxref\_neg DIODENWX AREA=4.45057e-12

+ PERIM=8.574e-06

XMMN0 N\_OUT\_MMN0\_d N\_IN\_MMN0\_g N\_GND!\_MMN0\_s N\_GND!\_D0\_noxref\_pos NFET L=7e-08

+ W=1.2e-06 AD=1.92e-13 AS=1.92e-13 PD=2.72e-06 PS=2.72e-06 NRD=0.0833333

+ NRS=0.0833333 M=1 NF=1 CNR\_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07

+ SB=1.6e-07 SD=0 PANW1=8.12e-15 PANW2=3.5e-15 PANW3=3.5e-15 PANW4=3.5e-15

+ PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14 PANW8=1.4e-14 PANW9=2.688e-14 PANW10=0

XMMP0 N\_OUT\_MMP0\_d N\_IN\_MMP0\_g N\_VDD!\_MMP0\_s N\_VDD!\_D0\_noxref\_neg PFET L=7e-08

+ W=1.7e-06 AD=2.72e-13 AS=2.72e-13 PD=3.72e-06 PS=3.72e-06 NRD=0.0588235

+ NRS=0.0588235 M=1 NF=1 CNR\_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07

+ SB=1.6e-07 SD=0 PANW1=7.63e-15 PANW2=3.5e-15 PANW3=3.5e-15 PANW4=3.5e-15

+ PANW5=3.5e-15 PANW6=7e-15 PANW7=4.446e-14 PANW8=2.473e-13 PANW9=5.6e-14

+ PANW10=7.637e-14

\*

.include "inv.pex.sp.INV.pxi"

\*

.ends

\*

\*

**Extracted Spice Netlist mt0 Screenshot**

